International
IOR Rectifier

80RIA SERIES

PHASE CONTROL THYRISTORS

Stud Version

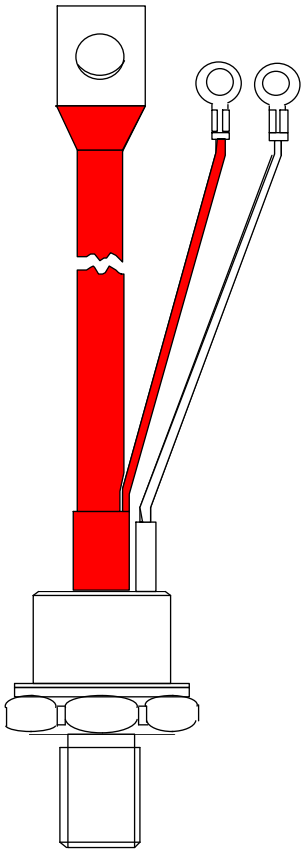
80A

Features

- All diffused design
- Glass-metal seal up to 1200V
- International standard case TO-209AC (TO-94)
- Threaded studs UNF 1/2 - 20UNF2A or ISO M12x1.75

Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers



case style
TO-209AC (TO-94)

Major Ratings and Characteristics

Parameters		80RIA	Unit
$I_{T(AV)}$		80	A
	@ T_C	85	°C
$I_{T(RMS)}$		125	A
I_{TSM}	@ 50Hz	1900	A
	@ 60Hz	1990	A
I^2t	@ 50Hz	18	KA^2s
	@ 60Hz	16	KA^2s
V_{DRM}/V_{RRM}		400 to 1200	V
t_q	typical	110	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM}, max. repetitive peak and off-state voltage V	V_{RSM}, maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ T_J = 125°C mA
80RIA	40	400	500	15
	80	800	900	
	120	1200	1300	

On-state Conduction

Parameter		80RIA	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	80	A	180° conduction, half sine wave		
	@ Case temperature	85	°C			
$I_{T(RMS)}$	Max. RMS on-state current	125	A	DC @ 75°C case temperature		
I_{TSM}	Max. peak, one-cycle non-repetitive surge current	1900	A	t = 10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max.
		1990		t = 8.3ms		
		1600		t = 10ms	100% V_{RRM} reapplied	
		1675		t = 8.3ms		
I^2t	Maximum I^2t for fusing	18	KA^2s	t = 10ms	No voltage reapplied	
		16		t = 8.3ms		
		12.7		t = 10ms	100% V_{RRM} reapplied	
		11.7		t = 8.3ms		
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	180.5	$KA^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied		
$V_{T(TO)1}$	Low level value of threshold voltage	0.99	V	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.		
$V_{T(TO)2}$	High level value of threshold voltage	1.13		(I > π x $I_{T(AV)}$),$T_J = T_J$ max.		
r_{t1}	Low level value of on-state slope resistance	2.29	mΩ	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.		
r_{t2}	High level value of on-state slope resistance	1.84		(I > π x $I_{T(AV)}$),$T_J = T_J$ max.		
V_{TM}	Max. on-state voltage	1.60	V	I_{pk}= 250A, T_J = 25°C t_p = 10ms sine pulse		
I_H	Maximum holding current	150	mA	T_J = 25°C, anode supply 12V resistive load		
I_L	Typical latching current	400				

Switching

	Parameter	80RIA	Units	Conditions
di/dt	Max. non-repetitive rate of rise of turned-on current	300	A/µs	T_J = 125°C, V_d = rated V_{DRM}, I_{TM} = 2xdi/dt snubber 0.2µF, 15Ω, Gate pulse: 20V, 65Ω, t_p = 6µs, t_r= 0.5µs Per JEDEC Standard RS-397, 5.2.2.6.
t_d	Typical delay time	1	µs	Gate pulse: 10V, 15Ω source, t_p = 6µs, t_r = 0.1µs, V_d = rated V_{DRM}, I_{TM} = 50Adc, T_J = 25°C.
t_q	Typical turn-off time	110		I_{TM} = 50A, T_J = T_J max, di/dt = -5A/µs min., V_R = 50V, dv/dt = 20V/µs, Gate bias: 0V 25Ω, t_p = 500µs

Blocking

	Parameter	80RIA	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	500	V/µs	T_J = 125°C exponential to 67% rated V_{DRM}
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	15	mA	T_J = 125°C rated V_{DRM}/V_{RRM} applied

Triggering

	Parameter	80RIA	Units	Conditions
P_{GM}	Maximum peak gate power	12	W	T_J = T_J max, $t_p \leq$ 5ms
$P_{G(AV)}$	Maximum average gate power	3		T_J = T_J max, f = 50Hz, d% = 50
I_{GM}	Max. peak positive gate current	3	A	T_J = T_J max, $t_p \leq$ 5ms
$+V_{GM}$	Maximum peak positive gate voltage	20	V	T_J = T_J max, $t_p \leq$ 5ms
$-V_{GM}$	Maximum peak negative gate voltage	10		
I_{GT}	Max. DC gate current required to trigger	270 120 60	mA	T_J = - 40°C T_J = 25°C T_J = 125°C Max. required gate trigger/ current/ voltage are the lowest value which will trigger all units 6V anode-to-cathode applied
V_{GT}	Max. DC gate voltage required to trigger	3.5 2.5 1.5	V	T_J = - 40°C T_J = 25°C T_J = 125°C
I_{GD}	DC gate current not to trigger	6	mA	T_J = T_J max Max. gate current/ voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied
V_{GD}	DC gate voltage not to trigger	0.25	V	

Thermal and Mechanical Specification

	Parameter	80RIA	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 150		
R_{thJC}	Max. thermal resistance, junction to case	0.30	K/W	DC operation
R_{thCS}	Max. thermal resistance, case to heatsink	0.1		Mounting surface, smooth, flat and greased
T	Mounting torque, ± 10%	15.5 (137)	Nm (lbf-in)	Non lubricated threads
		14 (120)		Lubricated threads
wt	Approximate weight	130	g	
	Case style	TO-209AC(TO-94)		See Outline Table

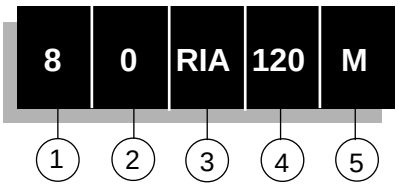
ΔR_{thJ-C} Conduction

(The following table shows the increment of thermal resistence R_{thJ-C} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.042	0.030	K/W	$T_J = T_J$ max.
120°	0.050	0.052		
90°	0.064	0.070		
60°	0.095	0.100		
30°	0.164	0.165		

Ordering Information Table

Device Code



1 - I_{TAV} x 10A

2 - 0 = Eyelet terminals (Gate and Auxiliary Cathode Leads)
1 = Fast - on terminals (Gate and Auxiliary Cathode Leads)
2 = Flag terminals (For Cathode and Gate Terminals)

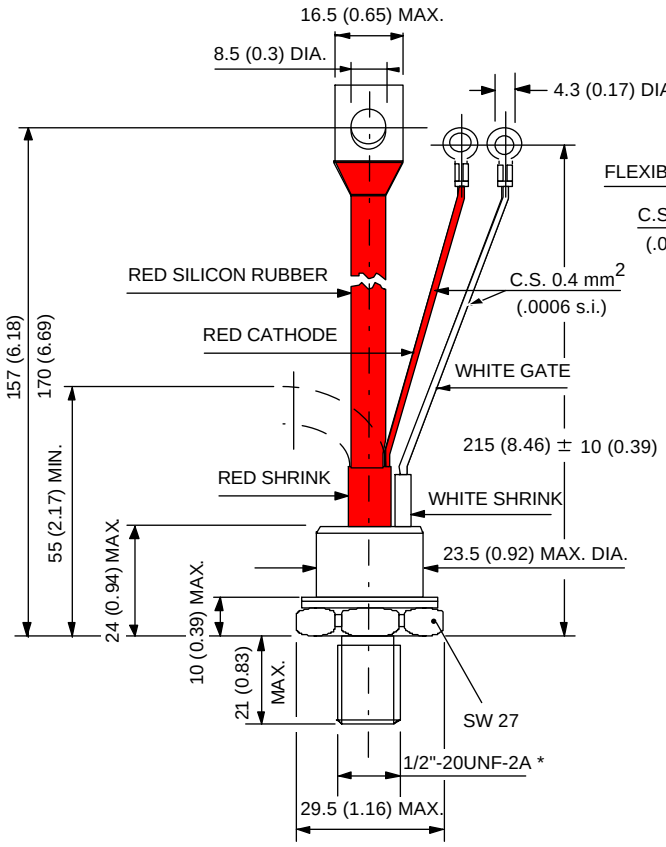
3 - RIA = Essential part number

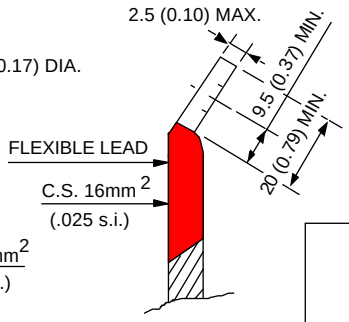
4 - Voltage code: Code x 10 = V_{RRM} (See Voltage Rating Table)

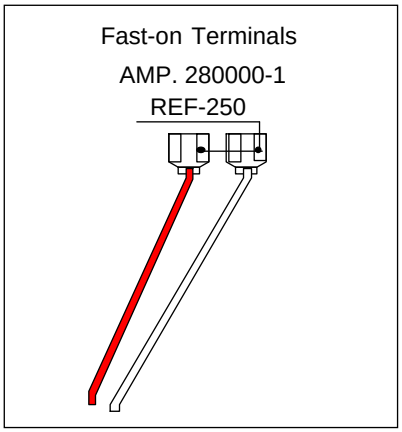
5 - None = Stud base 1/2 "20UNF - 2A threads
M = Stud base metric threads M12 x 1.75 E 6

Outline Table

GLASS METAL SEAL







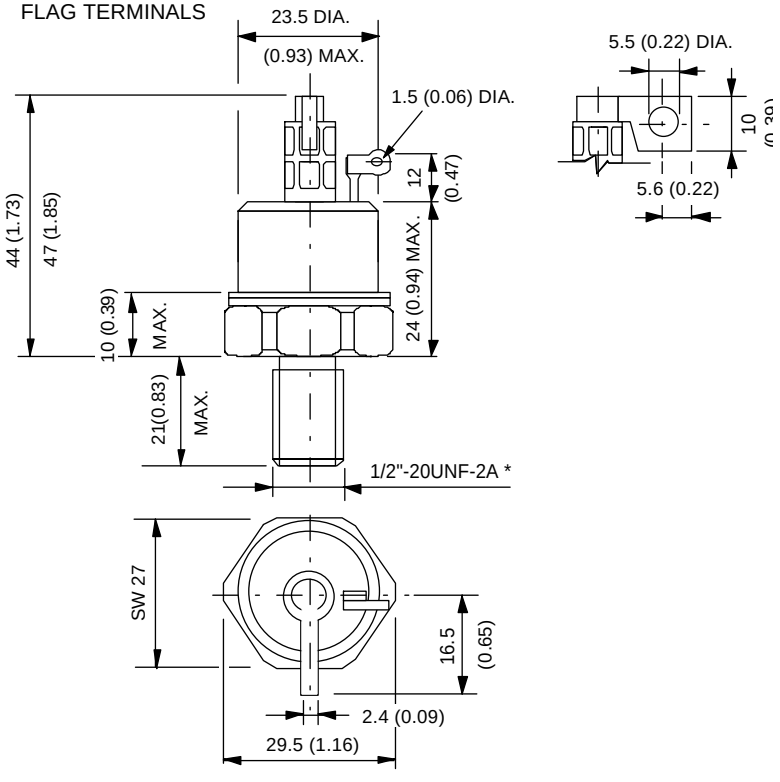
Case Style TO-209AC (TO-94)

All dimensions in millimeters (inches)

* FOR METRIC DEVICE : M12 x 1.75 E 6

GLASS-METAL SEAL

FLAG TERMINALS



Case Style TO-208AD (TO-83)

All dimensions in millimeters (inches)

* FOR METRIC DEVICE: M12 x 1.75 E 6

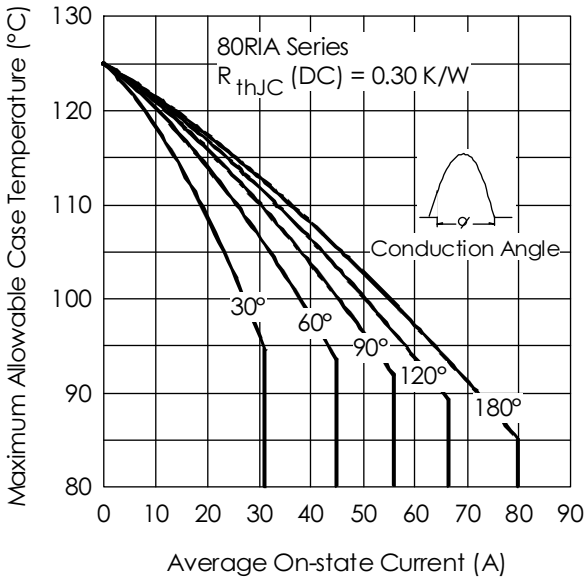


Fig. 1 - Current Ratings Characteristics

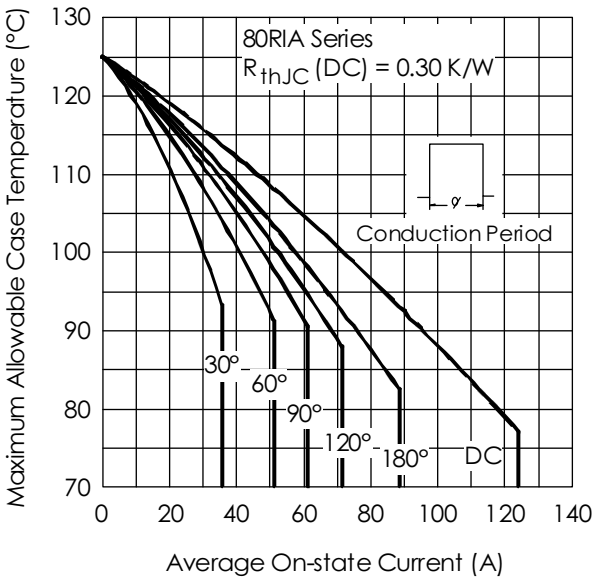


Fig. 2 - Current Ratings Characteristics

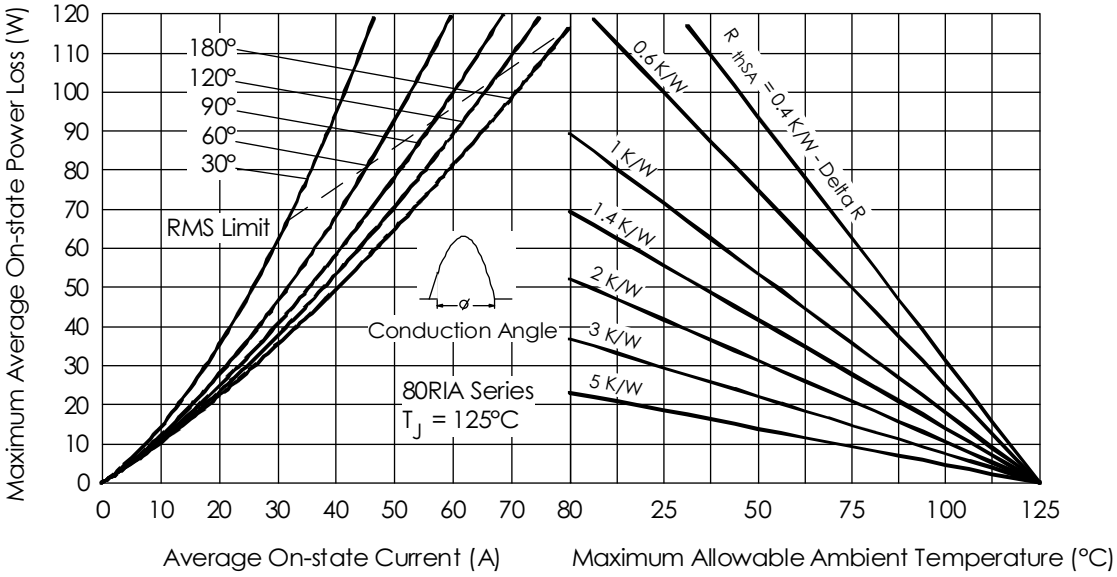


Fig. 3 - On-state Power Loss Characteristics

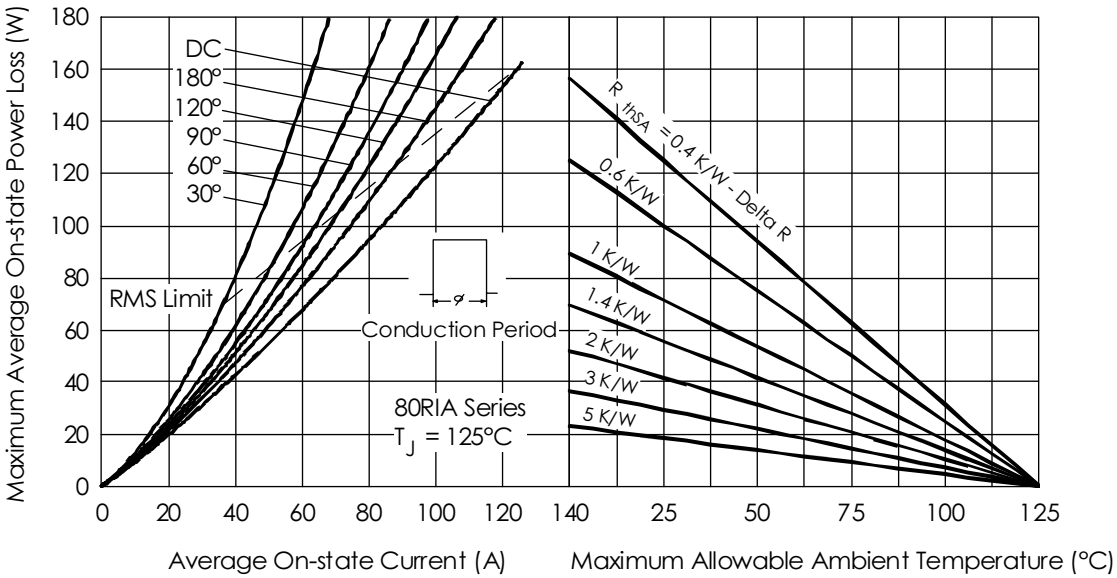


Fig. 4 - On-state Power Loss Characteristics

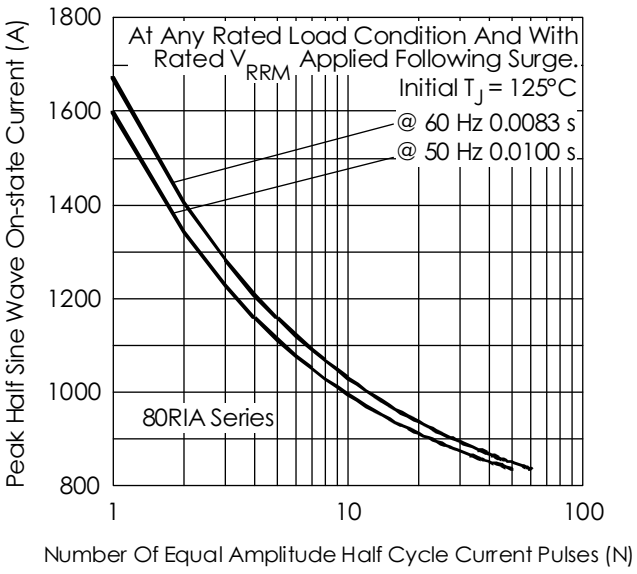


Fig. 5 - Maximum Non-Repetitive Surge Current

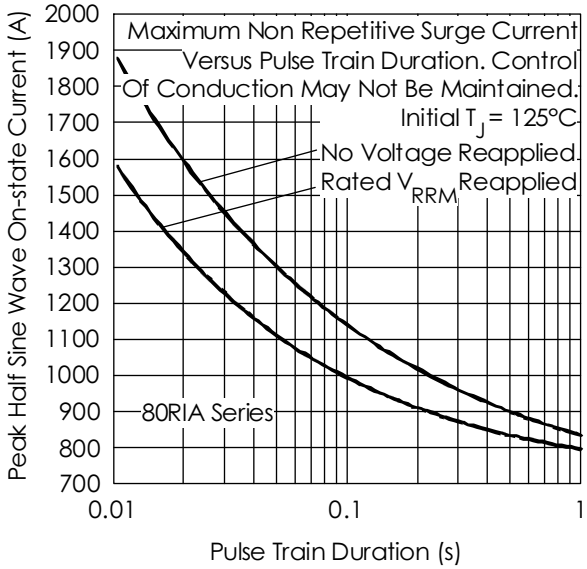


Fig. 6 - Maximum Non-Repetitive Surge Current

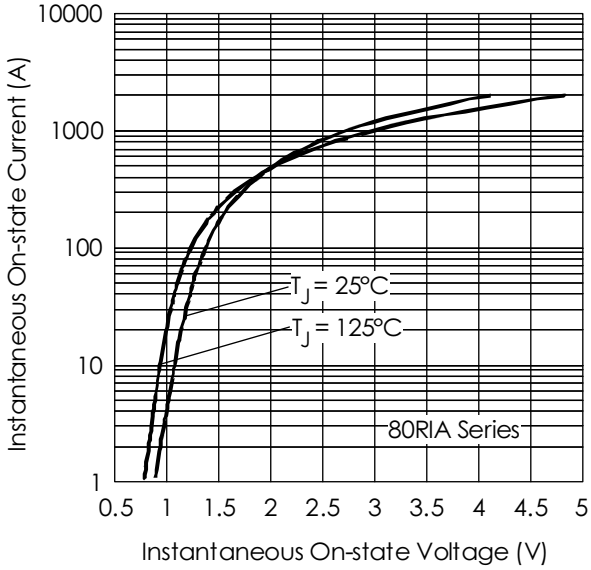


Fig. 7 - On-state Voltage Drop Characteristics

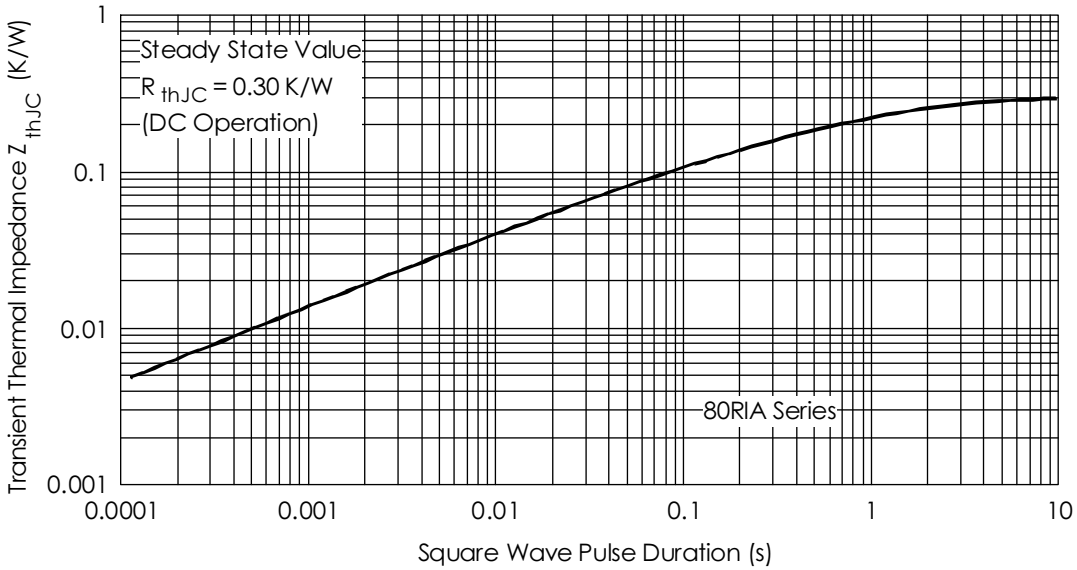


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

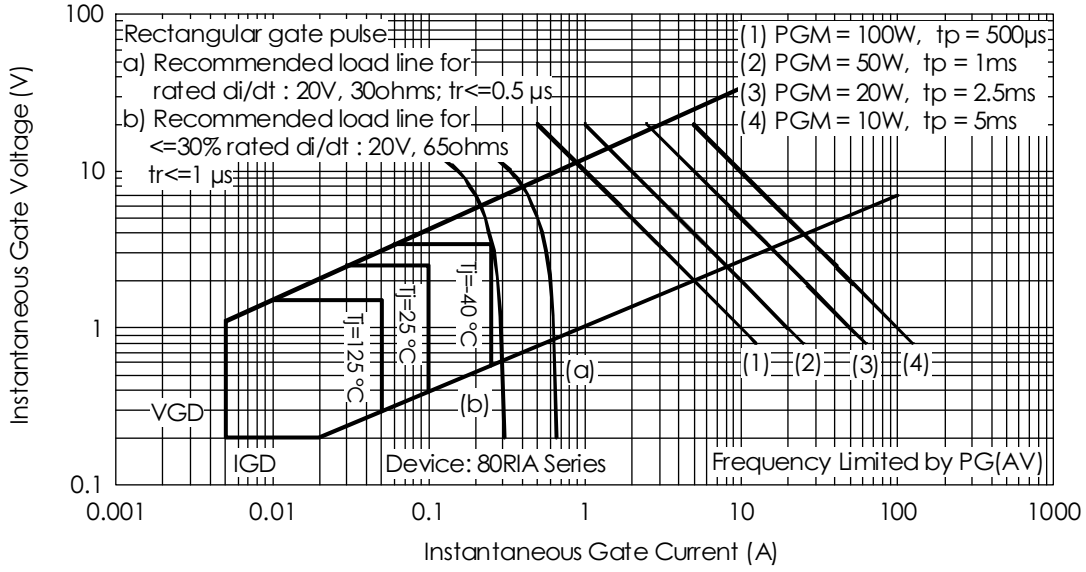


Fig. 9 - Gate Characteristics