

8.4A, 100V, 0.270 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09594.

Ordering Information

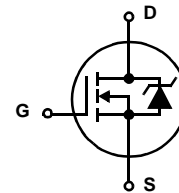
PART NUMBER	PACKAGE	BRAND
IRFR120	TO-252AA	IFR120
IRFU120	TO-251AA	IFU120

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in the tape and reel, i.e., IRFR120T.

Features

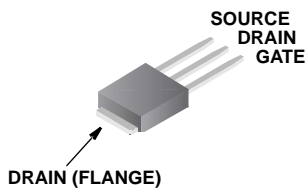
- 8.4A, 100V
- $r_{DS(ON)} = 0.270\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

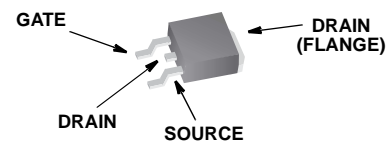


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



IRFR120, IRFU120

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFR120, IRFU120	UNITS
Drain to Source Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	100	V
Continuous Drain Current	8.4	A
$T_C = 100^\circ\text{C}$	5.9	A
Pulsed Drain Current (Note 3)	34	A
Gate to Source Voltage	± 20	V
Maximum Power Dissipation	50	W
Linear Derating Factor	0.33	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Figure 14)	36	mJ
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 10)	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_J = 150^\circ\text{C}$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10\text{V}$	8.4	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 500	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 5.9\text{A}$, $V_{GS} = 10\text{V}$ (Figures 8, 9)	-	0.25	0.27	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50\text{V}$, $I_D = 5.9\text{A}$ (Figure 12)	2.8	4.2	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 50\text{V}$, $I_D = 8.4\text{A}$, $R_{GS} = 18\Omega$, $R_L = 5.1\Omega$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	8.8	13	ns
Rise Time	t_r		-	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	19	29	ns
Fall Time	t_f		-	20	30	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}$, $I_D = 8.4\text{A}$, $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $I_{G(REF)} = 1.5\text{mA}$ (Figure 14) Gate Charge is Essentially Independent of Operating Temperature	-	9.7	15	nC
Gate to Source Charge	Q_{gs}		-	2.2	3.3	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	2.3	3.4	nC
Input Capacitance	C_{ISS}		$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 11)	-	350	-
Output Capacitance	C_{OSS}		-	130	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	24	-	pF
Internal Drain Inductance	L_D	Measured from the Drain Lead, 6.0mm (0.25in) from Package to Center of Die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6.0mm (0.25in) from Package to Source Bonding Pad	-	7.5	-	nH
		Modified MOSFET Symbol Showing the Internal Device Inductances				
Thermal Resistance, Junction to Case	$R_{\theta JC}$					
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Typical Solder Mount	-	-	110	$^\circ\text{C/W}$

IRFR120, IRFU120

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier	-	-	8.4	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	34	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 8.4\text{A}$, $V_{GS} = 0\text{V}$ (Figure 13)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 8.4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	55	110	240	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 8.4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	0.25	0.53	1.1	μC

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 25\text{V}$, starting $T_J = 25^{\circ}\text{C}$, $L = 770\mu\text{H}$, $R_G = 25\Omega$, Peak $I_{AS} = 8.4\text{A}$.

Typical Performance Curves Unless Otherwise Specified

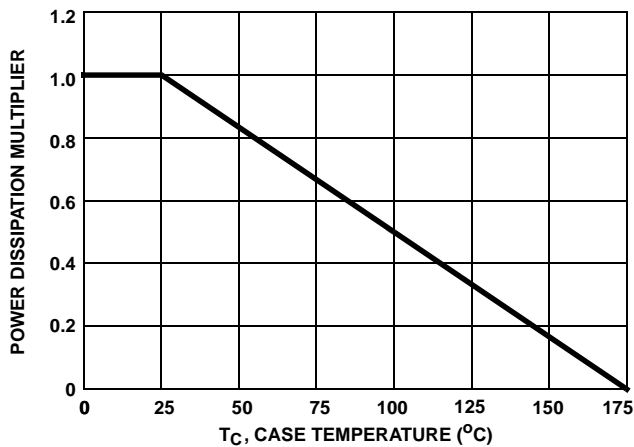


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

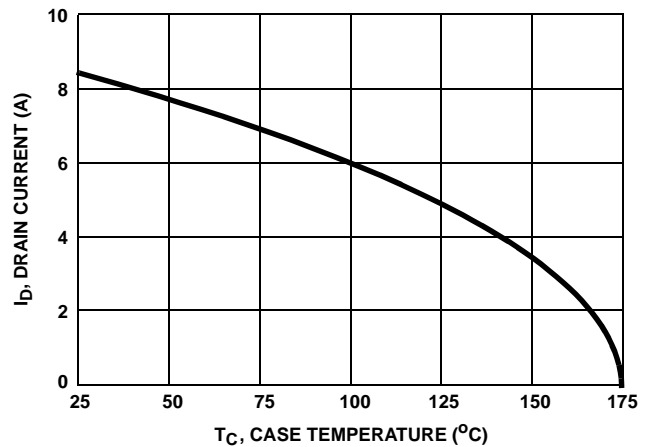


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

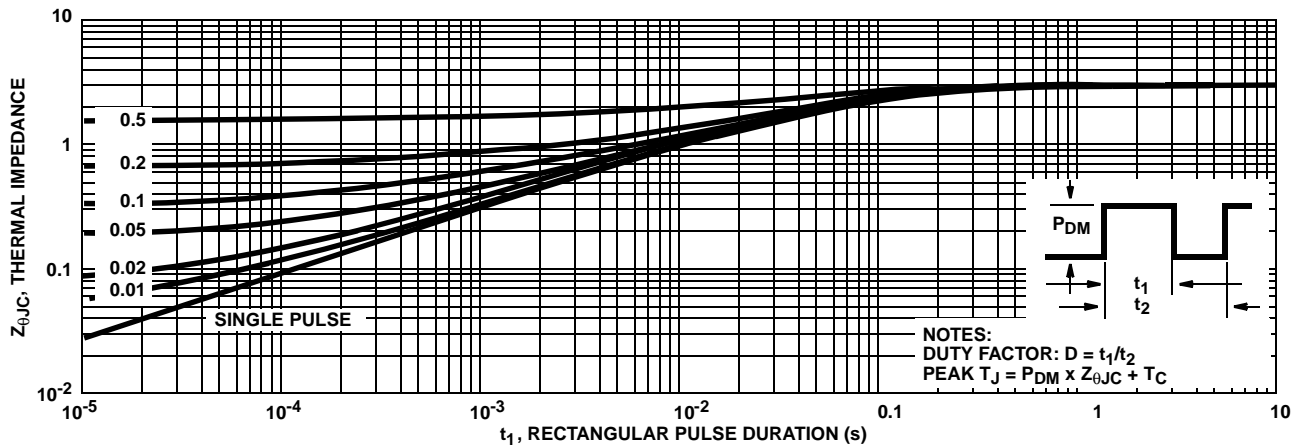


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

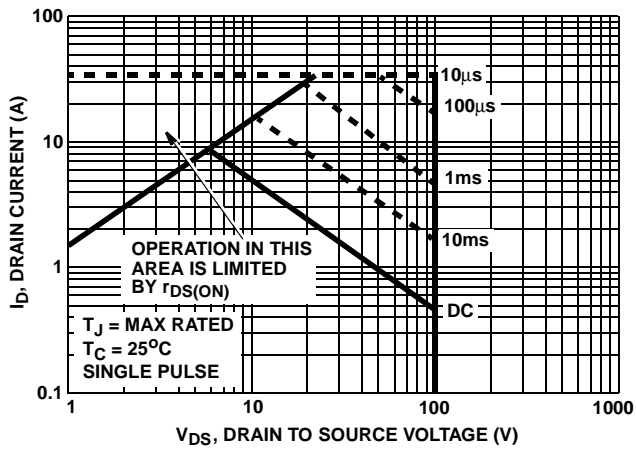


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

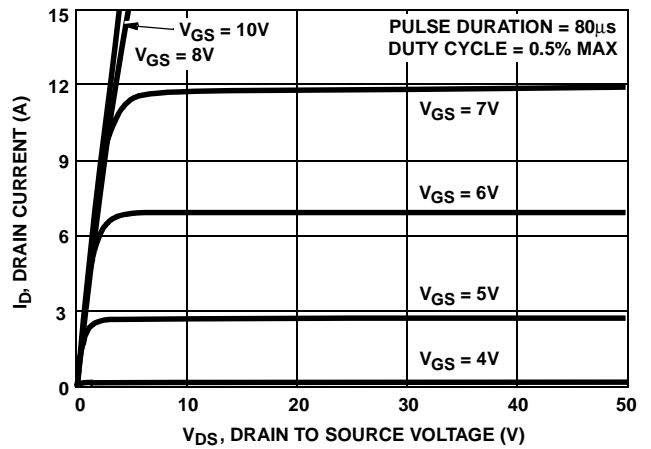


FIGURE 5. OUTPUT CHARACTERISTICS

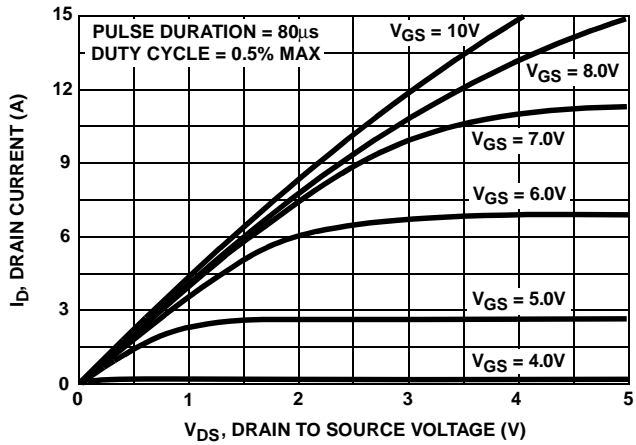


FIGURE 6. SATURATION CHARACTERISTICS

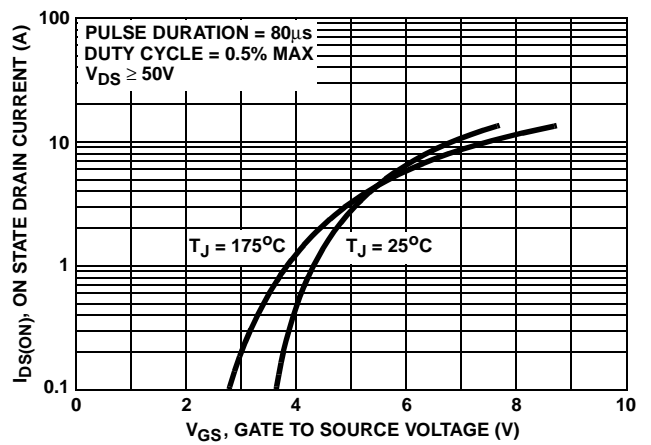


FIGURE 7. TRANSFER CHARACTERISTICS

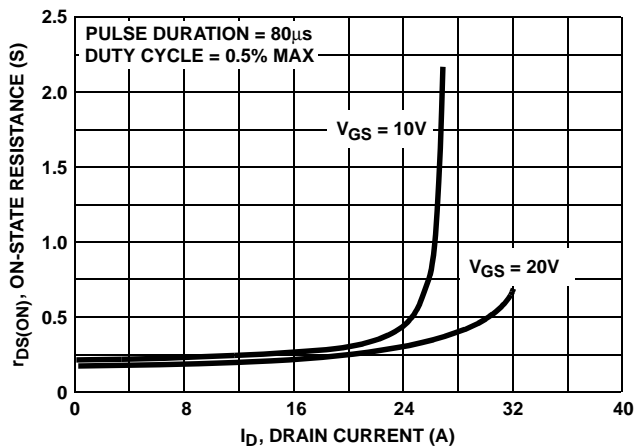


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

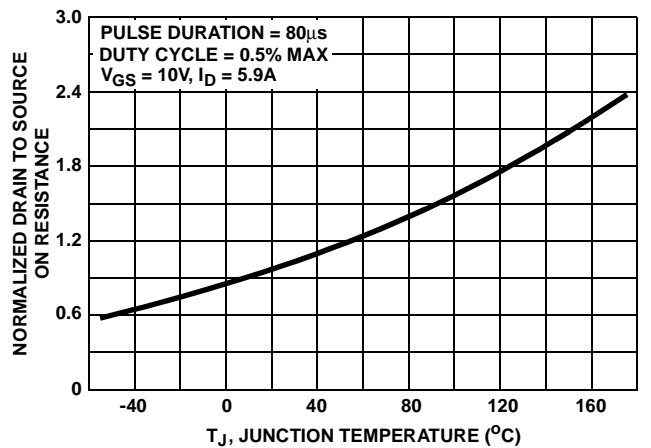


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

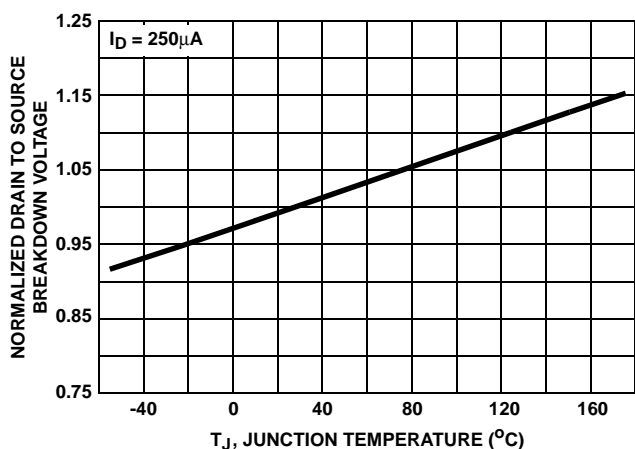


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

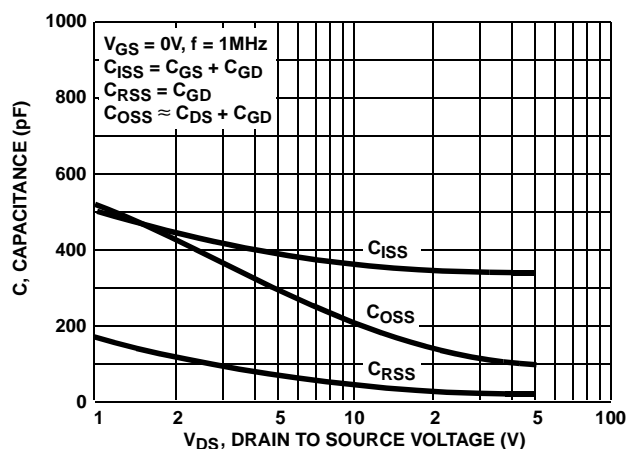


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

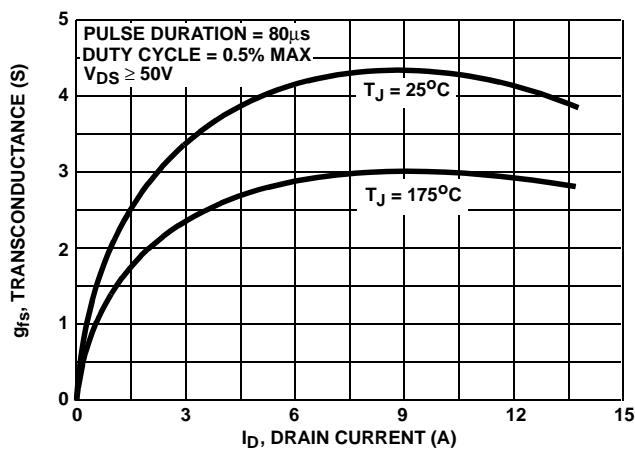


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

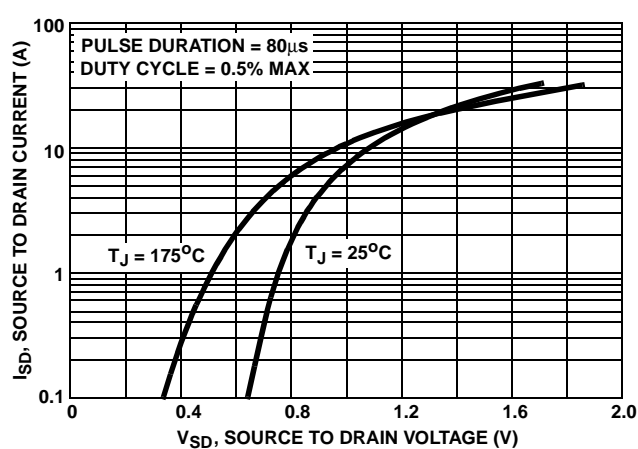


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

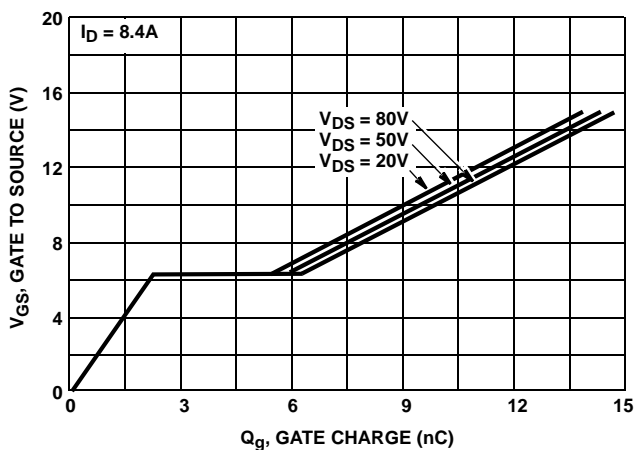


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

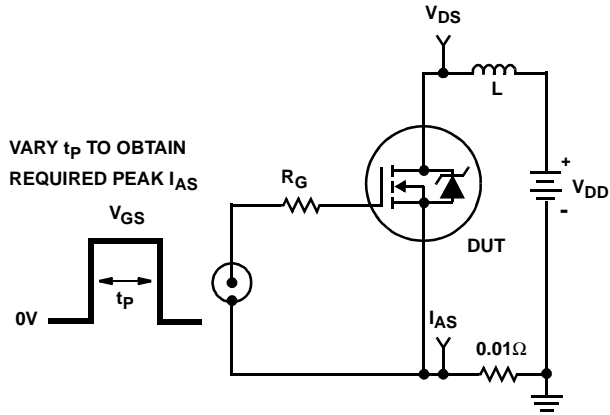


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

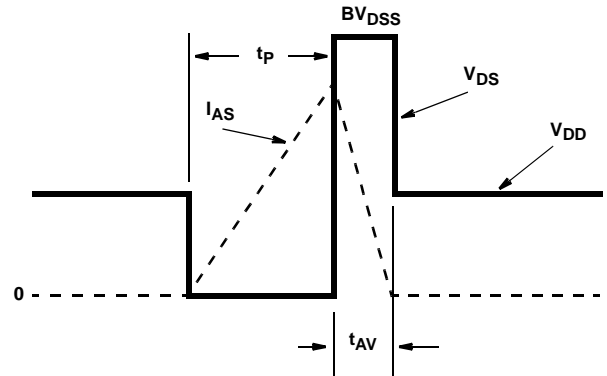


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

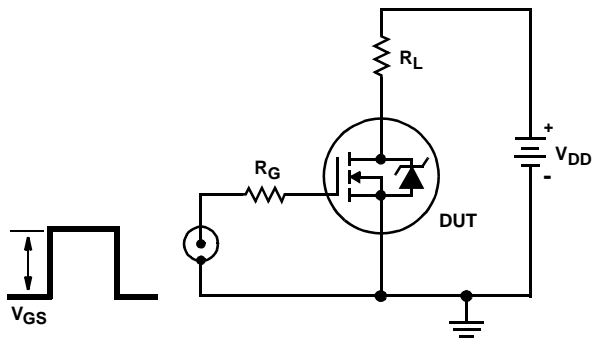


FIGURE 17. SWITCHING TIME TEST CIRCUIT

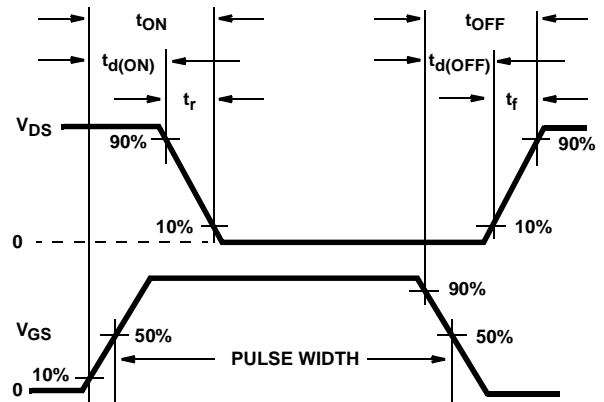


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

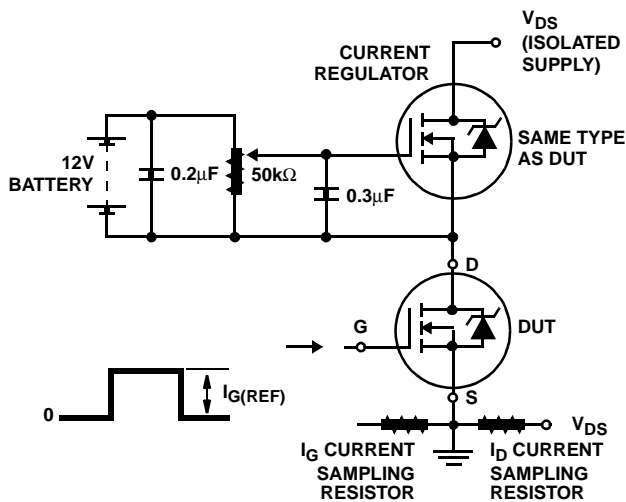


FIGURE 19. GATE CHARGE TEST CIRCUIT

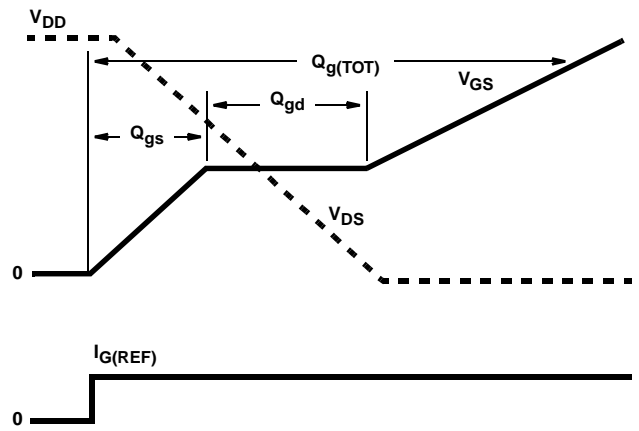


FIGURE 20. GATE CHARGE WAVEFORMS

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE _x TM	FAST [®]	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FAST _r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POPT TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOMET TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QST TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.