

IRL540N

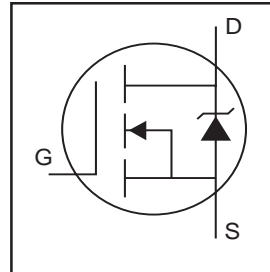
- Logic-Level Gate Drive
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

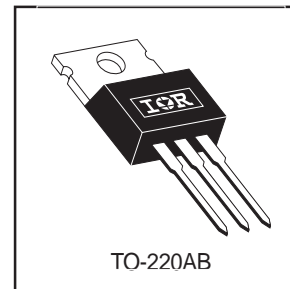
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

HEXFET® Power MOSFET



| |
|----------------------------|
| $V_{DS} = 100V$ |
| $R_{DS(on)} = 0.044\Omega$ |
| $I_D = 36A$ |



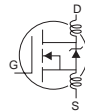
Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------|--|--------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 36 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 26 | |
| I_{DM} | Pulsed Drain Current ① | 120 | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 140 | W |
| | Linear Derating Factor | 0.91 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 16 | V |
| E_{AS} | Single Pulse Avalanche Energy② | 310 | mJ |
| I_{AR} | Avalanche Current① | 18 | A |
| E_{AR} | Repetitive Avalanche Energy① | 14 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.0 | V/ns |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | | |
| | Mounting torque, 6-32 or M3 screw | 10 lbf•in (1.1N•m) | |

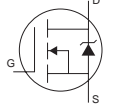
Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|-------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 1.1 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 62 | |

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|-------|---------------------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.11 | — | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.044 | Ω | $V_{GS} = 10V, I_D = 18A$ ④ |
| | | — | — | 0.053 | | $V_{GS} = 5.0V, I_D = 18A$ ④ |
| | | — | — | 0.063 | | $V_{GS} = 4.0V, I_D = 15A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 2.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 14 | — | — | S | $V_{DS} = 25V, I_D = 18A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 100V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 16V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -16V$ |
| Q_g | Total Gate Charge | — | — | 74 | nC | $I_D = 18A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 9.4 | | $V_{DS} = 5.0V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 38 | | $V_{GS} = 5.0V$, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 11 | — | ns | $V_{DD} = 50V$ |
| t_r | Rise Time | — | 81 | — | | $I_D = 18A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 39 | — | | $R_G = 5.0\Omega, V_{GS} = 5.0V$ |
| t_f | Fall Time | — | 62 | — | | $R_D = 2.7\Omega$, See Fig. 10 ④ |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | |  |
| C_{iss} | Input Capacitance | — | 1800 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 350 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 170 | — | | $f = 1.0\text{MHz}$, See Fig. 5 |

Source-Drain Ratings and Characteristics

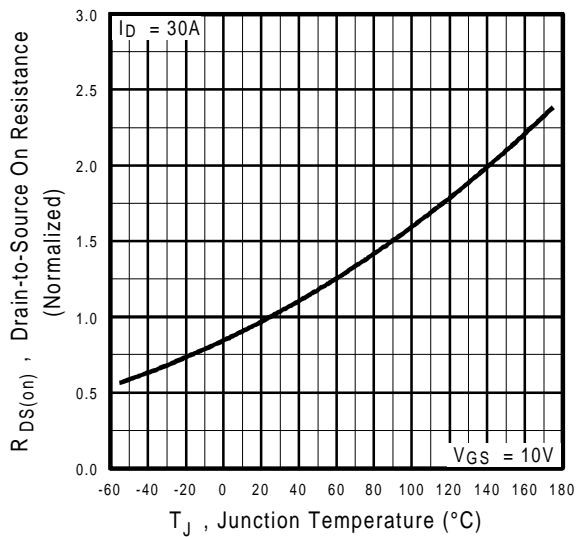
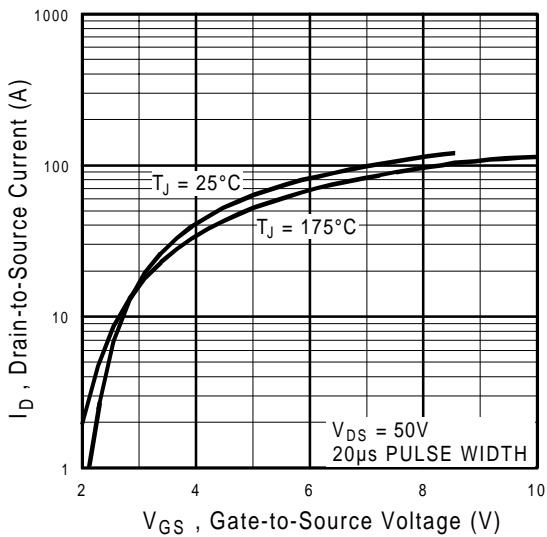
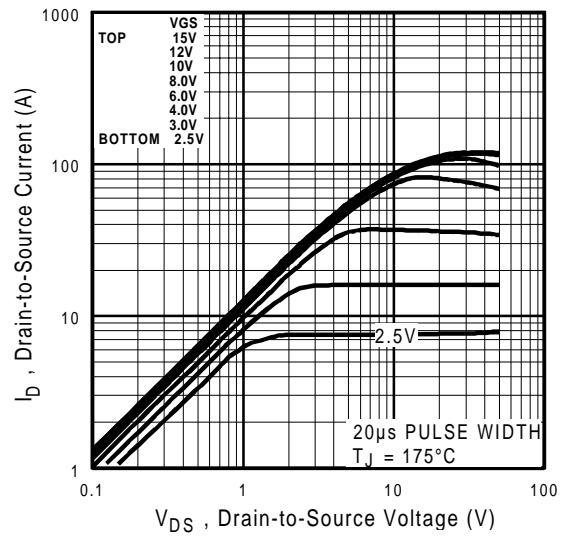
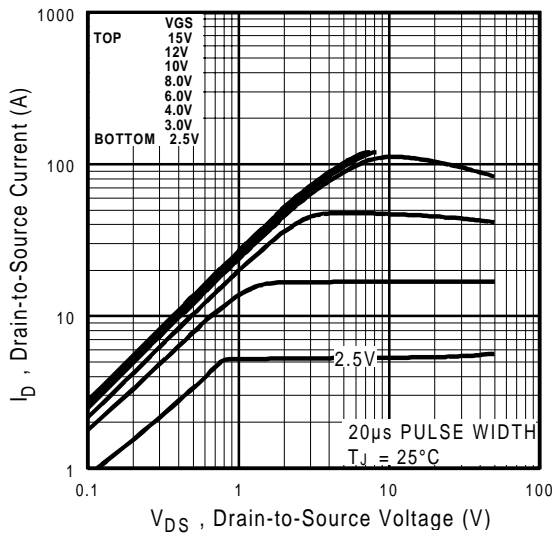
| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|---------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 36 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) ①⑥ | — | — | 120 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 190 | 290 | ns | $T_J = 25^\circ\text{C}, I_F = 18A$ |
| Q_{rr} | Reverse Recovery Charge | — | 1.1 | 1.7 | μC | $di/dt = 100A/\mu s$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 ② Starting $T_J = 25^\circ\text{C}, L = 1.9\text{mH}$
 $R_G = 25\Omega, I_{AS} = 18A$. (See Figure 12)

③ $I_{SD} \leq 18A, di/dt \leq 180A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$



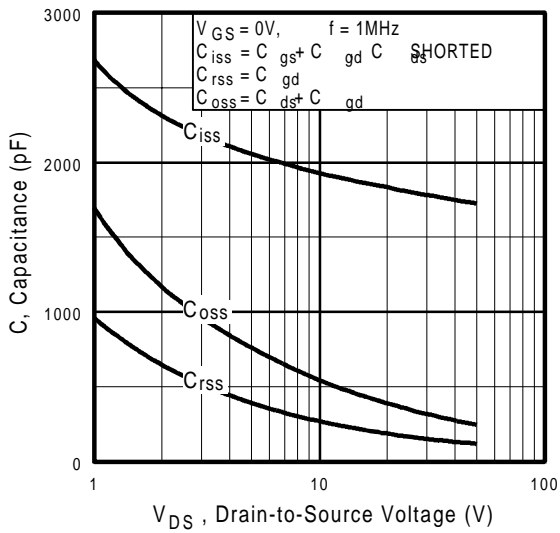


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

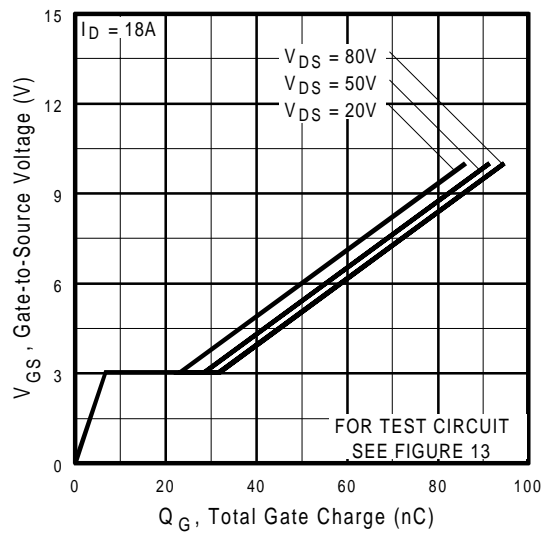


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

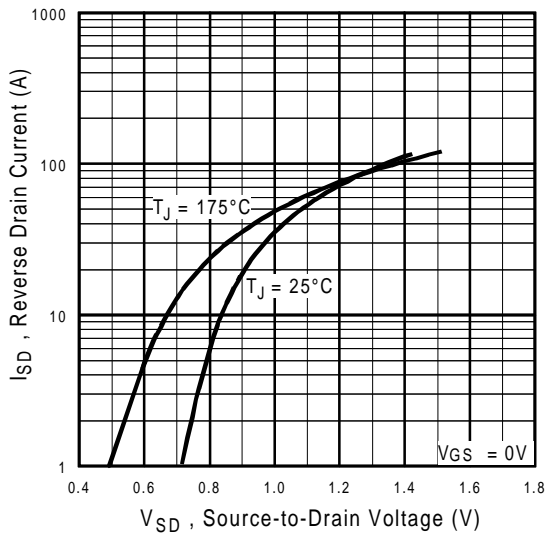


Fig 7. Typical Source-Drain Diode Forward Voltage

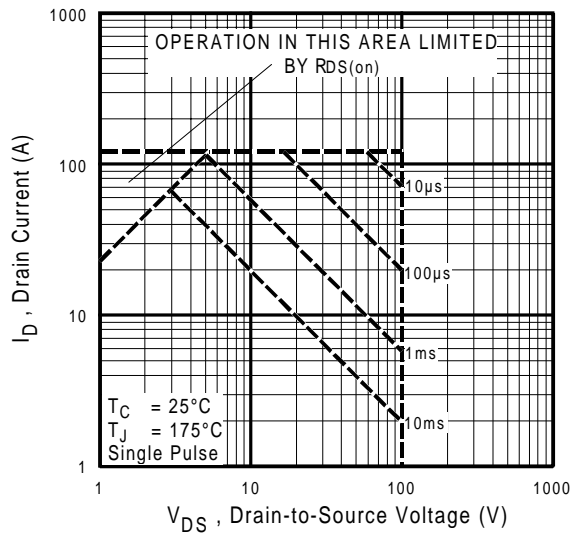


Fig 8. Maximum Safe Operating Area

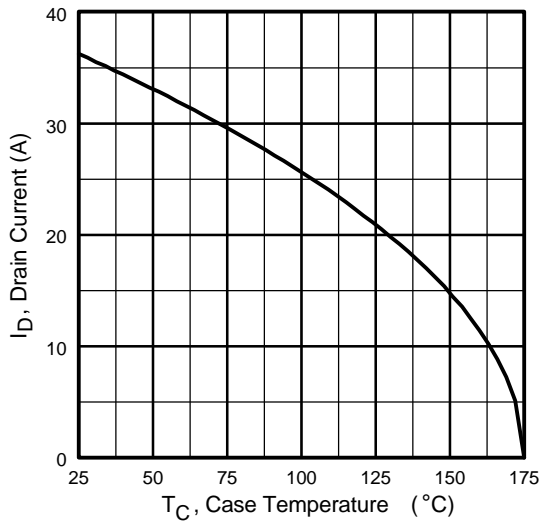


Fig 9. Maximum Drain Current Vs. Case Temperature

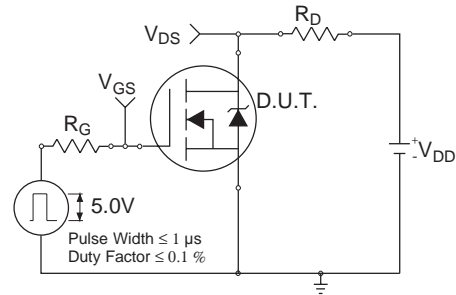


Fig 10a. Switching Time Test Circuit

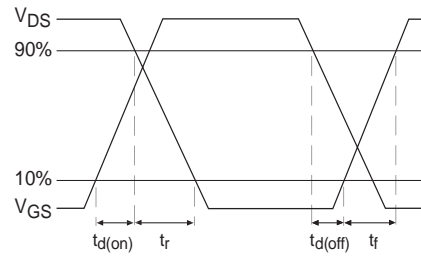


Fig 10b. Switching Time Waveforms

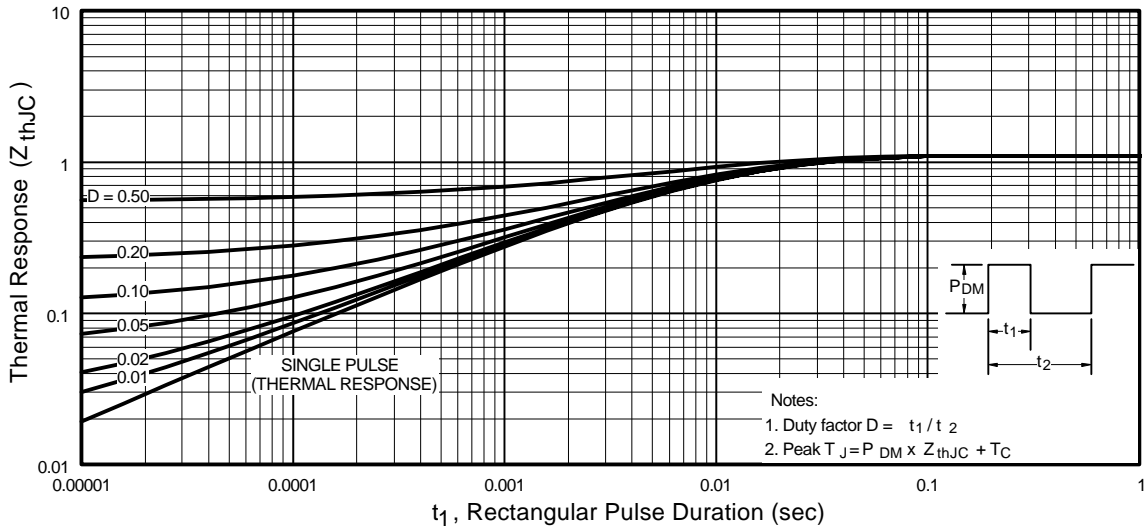


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

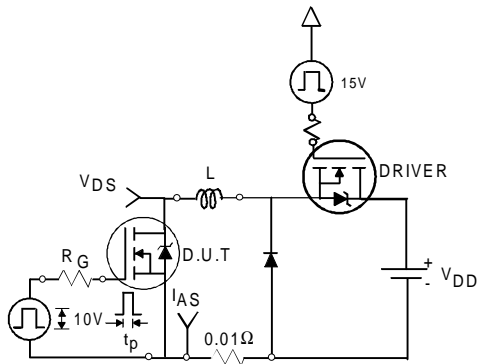


Fig 12a. Unclamped Inductive Test Circuit

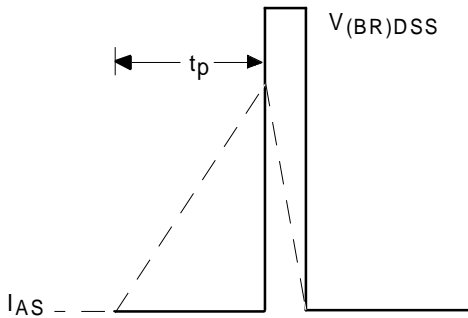


Fig 12b. Unclamped Inductive Waveforms

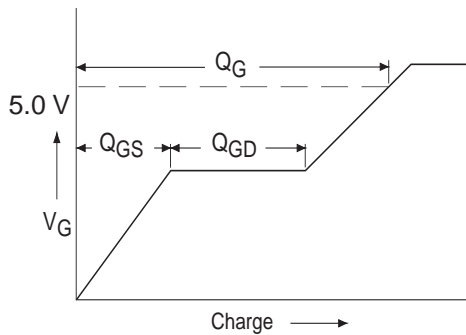


Fig 13a. Basic Gate Charge Waveform

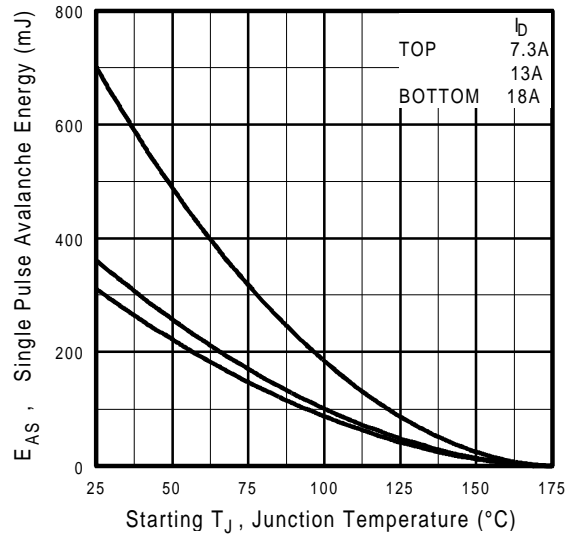


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

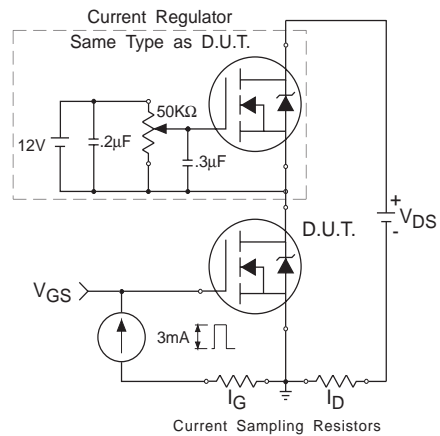
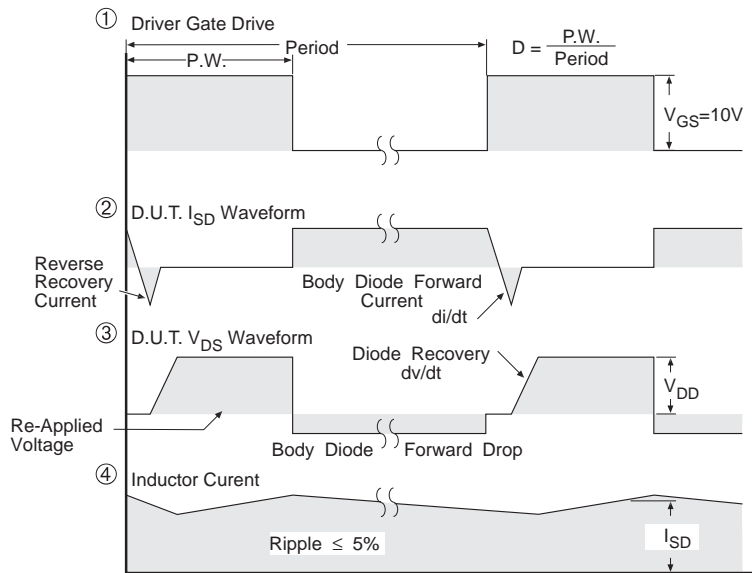
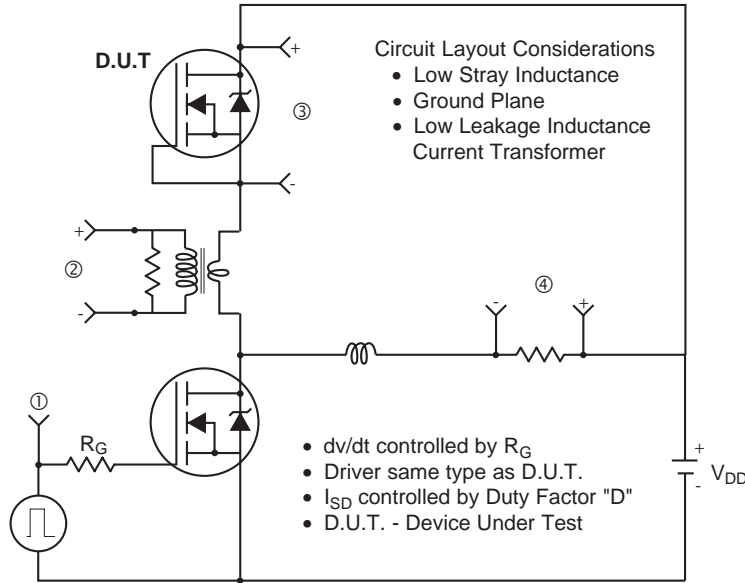


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

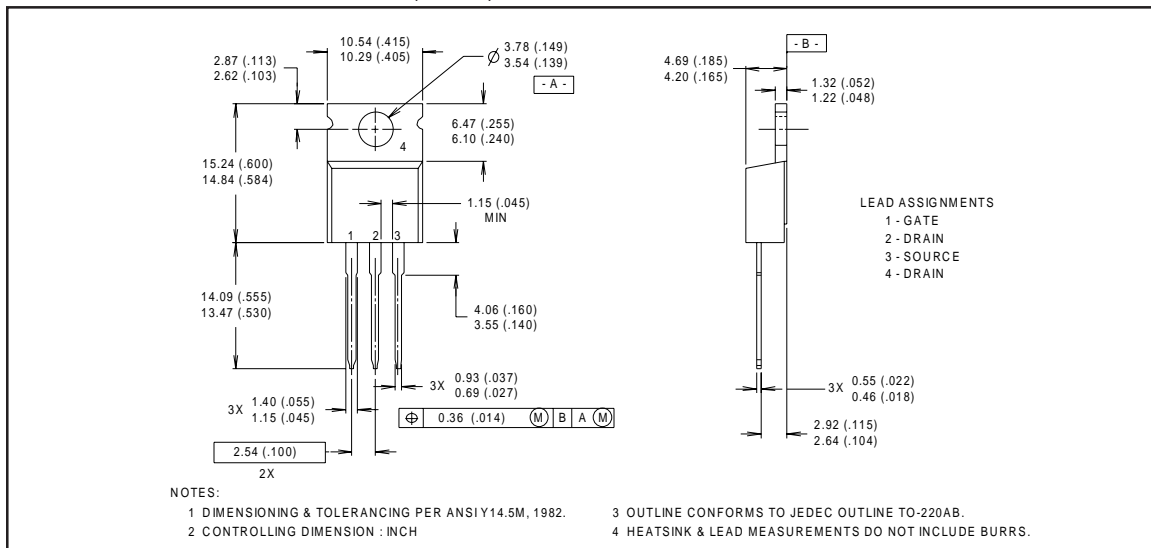
IRL540N

International
IR Rectifier

Package Outline

TO-220AB Outline

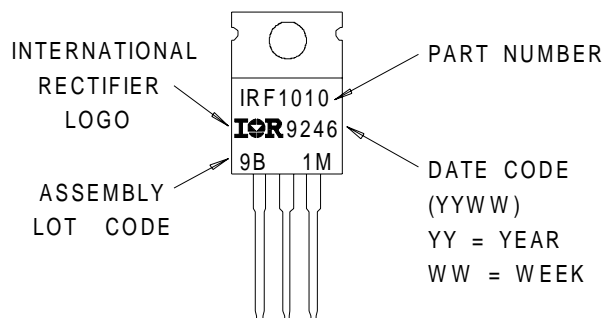
Dimensions are shown in millimeters (inches)



Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



International
IR Rectifier

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IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

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